IN THE CLAIMS:

Please amend claims 1-4 and add new claims 5-9 as follows.

1. (Currently Amended) A multi-port semiconductor memory comprising;

a memory cell array including a plurality of memory cells,

a first bit line pair performing write-in or read-out of complementary data for said ~~the~~ memory cells in said ~~the~~ memory cell array,

a second bit line pair performing write-in or read-out of complementary data for said ~~the~~ memory cells in said ~~the~~ memory cell array,

a plurality of first word lines provided for each of the memory cells for selecting a first ~~the~~ memory cell ~~that is accessed to the first bit line pair~~ from said ~~the~~ memory cell array,

a plurality of second word lines provided to ~~for~~ each of said ~~the~~ memory cells for selecting a second ~~the~~ memory cell ~~that is accessed to the second bit line pair~~ from said ~~the~~ memory cell array,

and a first pull-up circuit that, when data is written in said first ~~the~~ memory cell ~~that is selected~~ from said ~~the~~ first bit line pair, pulls up ~~a~~ low-level ~~side~~ of a lower-level line in said ~~the concerned~~ first bit line pair.

2. (Currently Amended) The multi-port semiconductor memory according to claim 1 further comprising a first regulator circuit that regulates lower power potential of said first ~~the~~ memory cell such that the pull-upped low-level in said ~~for the~~ first bit line pair ~~after pull-up~~ is written in said first ~~the~~ memory cell as low-level.

3. (Currently Amended) The multi-port semiconductor memory according to claim 1 or 2 further comprising a second pull-up circuit that, when data is written in said second ~~the~~ memory cell ~~that is selected~~ from said ~~the~~ second bit line pair, pulls up ~~a~~ low level

~~side~~ of a lower-level line in said ~~the concerned~~ second bit line pair.

4. (Currently Amended) The multi-port semiconductor memory according to the claim 3 further comprising a second regulator circuit that regulates lower power potential of said second ~~the~~ memory cell such that the pull-upped low-level in said ~~for the~~ second bit line pair ~~after pull-up~~ is written in said second ~~the~~ memory cell as low level.

5. (New) The multi-port semiconductor memory according to the claim 1, wherein said memory cell comprises:

flip-flop MOS transistors forming a flip-flop storing data, and

gate MOS transistors forming a gate between said flip-flop and said first bit line pair.

6. (New) The multi-port semiconductor memory according to the claim 2, wherein said memory cell comprises:

flip-flop MOS transistors forming a flip-flop for storing data, and

gate MOS transistors forming a gate between said flip-flop and said first bit line pair

wherein said first regulator circuit comprises MOS transistor for switching between said gate MOS transistors and a ground line.

7. (New) The multi-port semiconductor memory according to the claim 1, wherein said first pull-up circuit comprises:

a first MOS transistor having a source connected to one bit line in said first bit line pair, a drain connected to a power line and a gate inputted a write-in enable signal, and

a second MOS transistor having a source connected to another bit line in said first bit line pair, a drain connected to a power line and a gate inputted a write-in enable signal.

8. (New) The multi-port semiconductor memory according to the claim 3, wherein said second pull-up circuit comprises:

a first MOS transistor having a source connected to one bit line in said second bit line pair, a drain connected to a power line and a gate inputted a write-in enable signal, and

a second MOS transistor having a source connected to another bit line in said second bit line pair, a drain connected to a power line and a gate inputted a write-in enable signal.

9. (New) The multi-port semiconductor memory according to the claim 4, wherein said memory cell comprises:

flip-flop MOS transistors forming a flip-flop for storing data, and

gate MOS transistor forming a gate between said flip-flop and said first bit line pair

wherein said second regulator circuit comprises MOS transistor for switching between said gate MOS transistors and a ground line.